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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/431,477	11/01/1999	KIRAN GANESH	884.141US1	8764

21186 7590 09/25/2003

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MINNEAPOLIS, MN 55402

EXAMINER

KIK, PHALLAKA

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 09/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/431,477

Applicant(s)

GANESH ET AL.

Examiner

Phallaka Kik

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on RCE and amendment filed on 7/24/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-8,10-23,25-27 and 29-39 is/are pending in the application, *wherein claims 3,9,24,28 are cancelled.*
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 13-21 is/are allowed.
- 6) ☒ Claim(s) 1,2,4-8,10-12,22,23,25-27,29-33,38 and 39 is/are rejected.
- 7) ☒ Claim(s) 34-37 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 November 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/24/2003 has been entered.
2. Claims 1-2,4-8,10-23,25-27,29-39 are pending, wherein claims 3,9,24,28 were previously cancelled, claims 1,6-8,12-13,22,26,29,31 have been amended, and claims 32-39 have been newly added. Claims 1-2,4-8,10-23,25-27,29-39 have been examined, wherein claims 1-2,4-8,10-12,22-23,25-27,29-33,38-39 are newly rejected, claims 13-21 are allowed and claims 34-37 are objected to.

Drawings

3. The drawings filed on 11/1/1999 are acceptable under the new rules as being easily readable and scannable, as indicated in the previous Office Action.

Claim Objections

4. **Claims 34-37** are objected to because of the following informalities:

As per **claim 34**, "multiple layout clusters" (line 4) should be --multiple cluster layouts-- for proper antecedent basis.

As per **claim 35**, the claim should depend on claim 34 to provide antecedent basis for "the multiple cluster layouts" (line 3).

As per **claim 36**, the claim should depend on claim 34 to provide antecedent basis for the step of "assigning each transistor to a cluster" (line 1).

As per **claim 37**, the claim should depend on claim 34 to provide antecedent basis for the step of "generating a cluster layout" (line 1).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 1-2,4-8,10-12,22-23,25-27,29-33,38-39** are rejected under 35 U.S.C. 102(e) as being anticipated by **Scheffer et al.** (US Patent No. 6,543,041).

As per **claims 1,7,22,26,29,33,38,39**, all of the elements of the claims are illustrated in Figures 1 and 2, wherein the steps of receiving circuit design and reliability constraint are part of blocks 103 and 105, the generation/placement of circuit layout is part of block 204 and performing analysis is part of blocks 206 to 221 as illustrated in Figure 2, wherein block 212 performs the re-arrangement of the layout, which are

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performed repetitively until signal integrity and reliability constraints are satisfied (see also col. 2, line 52 to col. 3, line 53), wherein the cell library, the schematic design tool and the netlist tool are inherently part of the blocks 103, 105, 104, 106, 108, 109, necessary to create the proper circuit design specification and generating logic synthesis resulting in gate level netlist as is well known in the art, and wherein computer readable medium, processor, and instructions are further described in Fig. 6.

As per **claims 2,8,23,27**, the reliability verification for electro-migration is part of the hot electron problems considered (col. 3, line 65 to col. 4, line 4).

As per **claim 4**, the consideration of maximum current for a given wire width is also described in col. 4, line 63 to col. 5, line 9.

As per **claim 5**, since the method/apparatus of **Scheffer et al.** applies to all types of circuit design (col. 1, lines 6-12), the circuit design being a microprocessor design is within the scope of the invention.

As per **claims 6,11,25**, all of the elements of the claims are discussed in the rejection of claims 1,7,22, which the claims depend respectively, wherein the circuit layout is a two-dimensional layout comprising a plurality of overlapping rows are inherently included as part of the routing/placement problems that often occurs as is well known in the art.

As per **claims 10,12**, the consideration of density (i.e., current density or routing congestion), aspect ratio (i.e., gate re-sizing) and routing complexity (i.e., routing congestion or routing layers) are also described in col. 3, lines 58-63 and col. 4, line 63 to col. 5, line 27.

As per **claim 30**, the further routing tool corresponds to block 114 of Figure 1.

As per **claims 31-32**, all of the elements of the claims are discussed in the rejection of claims **1,7,22,26,29** above, wherein the self-heat and electromigration (i.e., hot electron) considerations are further described in col. 3, line 65 to col. 4, line 4.

Allowable Subject Matter

7. **Claims 13-21** are allowed.

8. **Claims 34-37** objected to as being dependent upon a rejected base claim, but would be allowable if claim 34 is rewritten in independent form including all of the limitations of the base claim and any intervening claims, and if claims 34-37 are rewritten or amended to overcome the objections due to minor informalities above set forth in this Office action.

9. The following is a statement of reasons for the indication of allowable subject matter:

As per **claims 13-21**, the independent claim 13, which the claims depend, recites the computerized method of placing a plurality of components of an integrated circuit in a layout, comprising the inventive steps/means for automatically rearranging the layout for the integrated circuit by automatically rearranging the plurality of clusters as claimed, which the prior arts made of record failed to teach or suggest. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

As per **claims 34-37**, claim 34, which claims 35-37 depend or should depend, recites the computerized method of creating a layout for a circuit design performed by a computer aided design tool, comprising the inventive steps/means for generating

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multiple cluster layouts that includes arranging the multiple cluster layouts, as part of the reliability verification-based repetitive performance and automatic rearrangement of the revised circuit layout as claimed, which the prior arts made of record failed to teach or suggest. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Remarks

10. The rejections of **claims 1-2,4,6-8,10-17,22-23,25-27,29-31** under 35 U.S.C. 102(b) as being anticipated by **Ito** (US Patent No. 5,648,910) are withdrawn in light of Applicant's amendment and arguments filed on 7/24/2003, wherein as pointed out by Applicant, **Ito** failed to teach the automatic re-arrangement of the circuit layout as claimed.
11. The rejections of **claims 1-2,4,6-8,10-17,22-23,25-27,29-31** under 35 U.S.C. 102(b) as being anticipated by **Hathaway et al.** (US Patent No. 5,737,580) are withdrawn in light of Applicant's amendment and arguments filed on 7/24/2003, wherein as pointed out by Applicant, **Hathaway et al.** failed to teach the automatic re-arrangement of the circuit layout as claimed.
12. The rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over **Ito** (US Patent No. 5,648,910) is withdrawn in light of Applicant's amendment and arguments filed on 7/24/2003, wherein as pointed out by Applicant, **Ito** failed to teach the automatic re-arrangement of the circuit layout as claimed.
13. The rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over **Hathaway et al.** (US Patent No. 5,737,580) is withdrawn in light of Applicant's

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amendment and arguments filed on 7/24/2003, wherein as pointed out by Applicant, **Hathaway et al.** failed to teach the automatic re-arrangement of the circuit layout as claimed.

14. As per **claims 1-12,22-33,38-39**, the claims are newly rejected under 35 U.S.C. 102(e) as being anticipated by **Scheffer et al.** (US Patent No. 6,543,041).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action. In particular, the following prior arts made of record are most relevant:

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 703-306-3039. The examiner can normally be reached on Flexitime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for
formal communications intended for entry,

Or:

(703) 746-4111 (for informal or draft communications, please label
"PROPOSED" or "DRAFT" and let the examiner know prior to faxing)
Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South
Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

**17. Applicant should note that effective May 1, 2003, the United States Patent
and Trademark Office has a new Commissioner for Patents address for
transitioning to the new Office location in Alexandria, VA, wherein
correspondence in patent-related matters to organizations reporting to the
Commissioner for Patents must now be addressed to:**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PK

September 6, 2003



**VUTHE SIEK
PRIMARY EXAMINER**